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JC3 SR3

U.S. UTILITY Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10021447	10/30/2001	702	125	2857	Bhat

2863

**APPLICANTS: Chan Siuki;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☒	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		X-885 US
Verified and Acknowledged Examiners's intials			

TITLE : Methods and circuits for measuring clock skew on programmable logic devices

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid	Primary Examiner	DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER	PREPARED FOR ISSUE	Application Examiner

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